

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	463197	(comput\$4 or calculat\$4 or determin\$5) near9 result\$3	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/12/19 10:25
L2	46944	(sequential\$3 or sequen\$4) and asynchronous	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/12/19 10:24
L3	55712	parallel near9 block\$3	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/12/19 10:24
L4	12711	phas\$3 near9 evaluat\$4	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/12/19 10:24
L5	468924	(comput\$4 or calculat\$4 or determin\$5) near9 output\$3	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/12/19 10:25
L6	13101	1 and 2	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/12/19 10:25
L7	1115	3 and 6	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/12/19 10:29
L8	44	4 and 7	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/12/19 10:26
L9	3	8 and input near9 (trigger or master)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/12/19 10:30
L10	6708	5 and 6	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/12/19 10:29
L11	32	2 and 3 and 4 and 5	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/12/19 10:30
L12	4	11 and input near9 (trigger or master)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/12/19 10:30

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- Drafts
 - BRS:
 - BRS:
- Pending
- Active
 - L1: (2) "6687725".pn.
 - L2: (2) "20040225699".pn.
 - L3: (122) multiplexer same phase same select \$4 same trigger
 - L4: (28) 13 and master
 - L5: (20) 13 and master and detect \$4
- Failed
- Saved
- Favorites
- Tagged (1)
- UDC
- Queue
- Trash

DB: US-PGPB USPA1 EPO-AO DERNERY, S3 Euse

Detail operator: OR Selected items only

13 and master and detect \$4

U	1	Document ID	IP	Title	Current	Current
1	2	US 6216254 B1		2. Integrated circuit design using a frequency synthesizer that automatically ensures testability	716/5	324/76
2	3	US 20050240352		2. Testing apparatus	714/740	
3	4	US 4660137 A		1. Circuitry for synchronizing a multiple channel circuit tester	714/760	
4	5	US 20040123167		2. System and method for interleaving point-of-load regulators	713/300	
5	6	US 4040028 A		1. Data processing system comprising input/output processors	710/36	
6	7	US 5301298 A		1. Method for utilizing a single multiplex address bus between DRAM, SRAM and ROM	710/313	710/35
7	8	US 20040225699		2. Method for early evaluation in micropipeline processors	708/233	
8	9	US 20030171903		2. Simulation and timing control for hardware accelerated simulation	703/16	
9	10	US 5404492 A		1. Head disk assembly simulator	703/13	369/31
10	11	US 4535409 A		1. Microprocessor based rscloser control	700/293	307/13
11	12	US 4771732 A		1. Non-invasive determination of mechanical characteristics in the body	600/587	600/55
12	13	US 6229365 B1		2. Phase difference detection circuit for liquid crystal display	375/375	327/23
13	14	US 6084930 A		2. Triggered clock signal generator	375/354	375/37
14	15	US 4134117 A		1. Loran C receiver	342/389	701/20
15	16	US 20040232395		2. Dual loop architecture useful for a programmable clock source and clock multiplier applic.	331/2	
16	17	US 4550232 A		1. Automatic oscillator frequency control system	331/2	331/1A
17	18	US 20040232997		2. Method and apparatus for temperature compensation	331/16	
18	19	US 5710517 A		1. Accurate alignment of clocks in mixed-signal tester	327/183	327/14
19	20	US 5457310 A		1. Method and system for automatically correcting boresight errors in a laser beam guidance	250/266	356/15
20		US 3835777 A		1. INK DENSITY CONTROL SYSTEM	101/350	101/36

Ready

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